UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,823,505 B1
DATED : November 23, 2004
INVENTOR(S) : Eric M. Dowling

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [63], **Related U.S. Application Data**, "Division of application No. 09/022,285, filed on Feb. 11, 1998, now Pat. No. 6,163,836." should read -- Divisional of application No. 09/022,285, filed on Feb. 11, 1998, now Pat. No. 6,163,836. --

Column 1,
Lines 24-26,
"The CICS architectures are being replaced by Reduced Instruction Set Computers (RISC) which are based on a simple load-store architecture. In a load-store architecture," should read -- The CISC architectures are being replaced by Reduced Instruction Set Computers (RISC) which are based on a simple load-store architecture. In a load-store architecture, --

Column 8,
Lines 14-16, "Program data is stored in the data memory 120 and carried by the data bus 112 which interconnects various elements, such as the MAC 116, the register set 102." should read -- Program data is stored in the data memory 120 and carried by the data bus 112 which interconnects various elements, such as the MAC 116 and the register set 102. --

Column 12,
Lines 25-27, "Table 3 list the code to compute the transpose address using a TMS320C2x to which the programmable AAU 350 has been added, as shown in FIG. 2. The code in Table 3 assumes" should read -- Table 3 lists the code to compute the transpose address using a TMS320C2x to which the programmable AAU 350 has been added, as shown in FIG. 2. The code in Table 3 assumes --

Column 14,
Lines 1-2, "500 can provided higher level combinatorial functions not provided by the cross-bar switch. The PLA 500 has sixteen" should read -- 500 can provide higher level combinatorial functions not provided by the cross-bar switch. The PLA 500 has sixteen --

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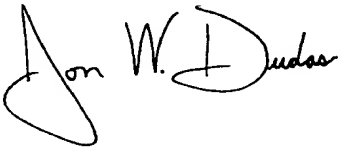
Column 17,
Lines 14-20, "writing a second program in a second programming language, said second program configured to implement a desired algorithm, wherein the second programming language comprises a fixed set instructions that make use of a fixed set of addressing modes, wherein at least one of the addressing modes comprises a user defined addressing mode:" should read -- writing a second program in a second programming language, said second program configured to implement a desired algorithm, wherein the second programming language comprises a fixed set of instructions that make use of a fixed set of addressing modes, wherein at least one of the addressing modes comprises a user defined addressing mode; --

Column 21,
Lines 7-14,
"a first software module comprising a collection of opcodes assembled from a fixed assembly language that has a fixed set of instructions, a fixed set of fixed addressing modes, and at least one user-defined auto-update addressing mode, wherein the execution of the first software module results in the implement an application algorithm through a sequence of individual op-code executions defined by a program flow; and" should read --a first software module comprising a collection of opcodes assembled from a fixed assembly language that has a fixed set of instructions, a fixed set of fixed addressing modes, and at least one user-defined auto-update addressing mode, wherein the execution of the first software module results in the implementation of an application algorithm through a sequence of individual op-code executions defined by a program flow; and --

Signed and Sealed this

Tenth Day of May, 2005



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